Effects of DC Bias on Multi-Layer Ceramic *Capacitors*

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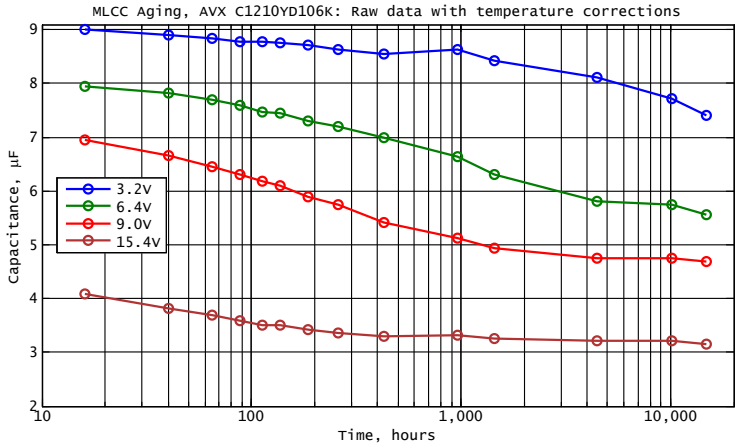
The word "capacitors" is highlighted in the title because Multi-Layer Ceramic Capacitors (MLCCs for short) can be rather poor approximations to an ideal capacitor. To the point in fact, that circuits may be unwittingly designed with inadequate margins. This is true in particular of high-value parts in small packages.

Experiments with a sample of MLCCs under varying levels of constant DC bias for more than 1-½ years reveal behavior that many seasoned engineers would find surprising. Those wonderfully small high-valued surface mount parts can lose a lot of their nameplate capacitance under bias and may continue losing even more if that bias is applied for a long period of time.



The graph above shows the results we found for 10μF 16-volt rated MLCCs in a 1210 surface mount package. Note the red curve which represents a bias level of 9 volts. On initial application of bias, capacitance is only 70% of the

10μF nameplate value, but after about 1,400 hours under bias it has dropped to less than half of the rated value.

1 Preliminaries

This article concerns capacitors manufactured using X7R and X5R dielectrics, which use ceramics containing barium titanate ($BaTiO_3$). Well-behaved Class I dielectrics (C0G, C0H, C0K) are not explored here, nor are more temperature sensitive dielectrics such as Y5V.

An ideal capacitor is defined by the differential equation

$$I = C\,\frac{dV}{dt}$$

where C is a constant. With MLCCs however, the value of C is not really a constant, but can vary a *lot* as a function of voltage and time. In other words,

$$C = C(V(t), t)$$

Experiments to explore this dependence revealed an important behavior we were previously unaware of, and it's something most circuit designers would want to know. This discovery was a big surprise and fundamentally changed the way we view MLCCs as a circuit component.

In what follows, three important aspects of MLCCs are discussed. Two are generally known; the third, not so much.

1. C decreases over time, even in storage (generally known).
2. C can vary strongly with applied voltage (generally known).
3. C decreases faster over time when biased (generally not known).

The last two issues listed above are associated with MLCCs which can be charged to very high levels of energy density. Although there doesn't seem to be an exact threshold for this, the last two issues seem to arise when MLCC energy density moves into a range of $2 - 13\mu\text{J/mm}^3$. Recommendations for avoiding these issues are provided later in the article. For those interested in the physical mechanisms responsible for these behaviors, references are provided in the bibliography.

High Density MLCCs In this article, the term *high density* should be understood to mean X5R and X7R MLCCs operated at energy densities above an approximate threshold range of $2 - 13\mu\text{J/mm}^3$.

Active Dielectric Volume The total volume of an MLCC is easily computed. The fraction of this volume which is biased dielectric is proprietary and can only be guessed at. This would require knowledge of internal construction which is not publicly available. Computing energy density from total MLCC volume is going to be inaccurate, and this may account for some of the fuzziness of the threshold range specified above.

An article published in 2007[8] shows some trends in layer counts, inactive part margins and the ratio between dielectric and electrode thickness. Although interesting, this doesn't really provide enough information to make accurate estimates of active dielectric volumes in various parts.

Aging vs Fatigue Loss of capacitance over time with zero applied bias is called *aging*. When bias is applied, loss may accelerate; this is sometimes referred to as *fatigue*. In some of the literature, *fatigue* refers to situations where mechanical stress is applied to a piezoelectric device. In this article, *fatigue* will refer to behavior under a constant DC bias.

The rate at which capacitance is lost due to fatigue in high density MLCCs can depend strongly on the applied bias. Our measurements lead us to believe that some high density MLCCs could lose half (or more) of their initial biased capacitance after being biased for long periods of time. This could be one plausible cause of long term "wearout" failures in modern electronic equipment.

Is Fatigue A Secret?

Manufacturers don't tell customers much about fatigue in MLCCs, even though it can be a critical factor in long lifetime designs. By way of an example, the Kemet company published a technical paper[9] which mainly focuses on loss of capacitance due to DC bias. It also discusses the aging process (see their figure 17), stating that MLCCs using X7R dielectric age at a rate of 2% per decade. There is little or no discussion of higher rates under bias, but our measurements show that this can be substantial and should not be ignored. This criticism is not unique to Kemet and we are not singling them out. This is just one example. We know of no MLCC manufacturer which publicly discusses fatigue behavior in any detail.

Second hand information leads us to suspect that MLCC manufacturers are well aware of this phenomena but many (or most) choose not to share it with customers. We also understand that at least some of them will admit

to this behavior if pressed. However, unless you work for a large corporation which spends a lot of money on capacitors, you may find it impossible to even speak with one of the manufacturers' representatives about this.

Whatever the case, we are puzzled by the lack of public information and guidance for designers on this topic. It can be a big deal, and no manufacturer is immune to it – they all use barium titanate as a major component of X5R and X7R dielectrics. In our opinion, they are doing their customers a disservice by keeping it under wraps.

We doubt there is much difference between manufacturers with regards to fatigue behavior, so this wouldn't seem to be a motive to keep quiet about it. If fatigue behavior was widely known however, engineers might shy away from high density MLCCs, choosing instead other technologies which are more stable over long periods of time under bias, such as solid polymer aluminum capacitors. Perhaps this could be a motive for keeping quiet about fatigue.

In summary we do not have direct evidence that manufacturers are intentionally hiding this behavior, even though it seems that way. Some of them may include at least some of the losses due to fatigue in their data regarding capacitance versus DC bias. In any case, we feel that manufacturers do, at a minimum, understate the importance of fatigue in high density MLCCs.

Minimal Acknowledgment of Fatigue

Here are two examples where manufacturers sort of, directly or indirectly admit that fatigue is an issue. First, AVX has the following single sentence in their MLCC catalog regarding fatigue:

> *Change in the aging curve can be caused by the application of voltage and other stresses.*

In our opinion, this is grossly inadequate because "*change in the aging curve*" can be quite large and zero indication of this is provided.

Figure 1 is from Kemet's K-Sim simulator and depicts capacitance versus DC bias for a 10μF 50V 1210 MLCC with X5R dielectric. Notice the abrupt change in slope at 10V bias. A bias sweep on the capacitor does not contain any abrupt changes in slope, and we suspect this may be an attempt to include the effects of fatigue at higher bias levels. See discussion of figure 13 in the text below for a bit more on this.

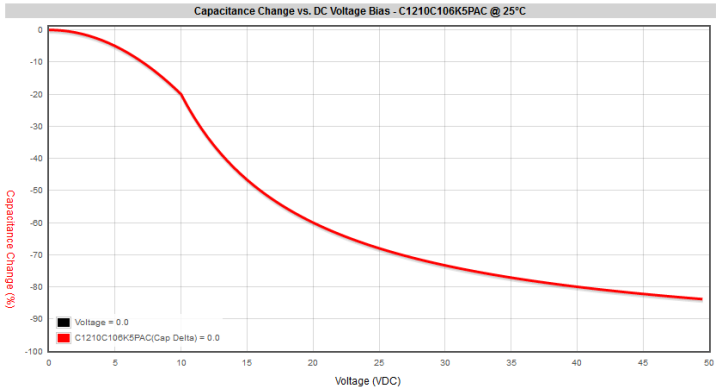


Figure 1: Kemet K-Sim output for 10uF 50V 1210 MLCC

It's Reversible

Mechanisms for aging and fatigue are known, and the net result is the same in both cases. Much of the research on fatigue in ceramic ferroelectrics is found in the field of piezoelectrics where barium titanate is also used.

Loss due to aging and fatigue can be reversed by heating the parts to a temperature above the Curie point of $BaTiO_3$. Heating MLCC capacitors to 150C (300F) for a couple of hours is sufficient to reverse the aging process. We used this technique to "reset" or "anneal" capacitors before beginning test runs. It's worth noting that the reflow soldering process for printed circuit boards does not typically apply heat for a long enough period of time to fully anneal MLCC capacitors.

While this annealing process is feasible for unmounted capacitors, and even for some assembled printed circuit boards (if all the other parts can withstand 150C), it's usually not practical for finished products. How would that look in an instruction manual, if the user was asked to place the device in an oven at 300F for a couple hours once a year?

FYI, don't try this at home in a cooking oven. A gas oven set to 300F can easily reach temperatures of 400F or more briefly during the temperature cycles and we've seen PCBs destroyed by attempting this. Electric range ovens might be different but we've not had any experience with them.

Our annealing is done in a toaster oven which has been fitted with a platinum RTD temperature probe, with the heating elements driven by a commercial PID controller.

Harmful Effects

Here is an incomplete listing of problems which could result if a capacitor is reduced in value excessively in a functioning circuit. You can probably think of more.

- Degradation of power supply de-coupling may result in:
  - A slow increase in noise or decrease in sensitivity specs over time.
  - Malfunctions in digital circuits with poor noise margins.
  - Failure to meet various specifications.
- Some power supply designs require a minimum amount of load capacitance for stability. Reduced capacitance may cause power supplies to become unstable and go into oscillation.
- Analog circuits can go out of spec or become unstable.
- Problems may occur where MLCCs are used to guarantee a short amount of system operating time after a power failure.

The last bullet item above is motivated by the design of an embedded system, in which power supply capacitance was sized to provide operating voltage for a processor to write data to flash memory after sensing a power failure. If capacitance drops too much there would be inadequate time to accomplish that task, and flash memory could become corrupted.

Aging

We're told that aging occurs linearly with logarithmic time. This statement may be found just about anywhere MLCC aging is discussed, including most manufacturers' web sites. This means that for every ten-fold increase in time a certain percentage of the original capacitance is lost. *Log-time* can be defined as

$$x(t) = \log_{10}\left(\frac{t}{t_o}\right)$$

A typical specification is 2 or 3% per decade of time. There seems to be an industry agreement that MLCCs should be within the rated tolerance after

storage for 1,000 hours (about 42 days). This behavior can be expressed as an equation:

$$C(t) = C_o \left[\ 1 - ax(t)\ \right]_{t \geq t_o},$$

where C_o is the capacitance at time t_o and a defines the amount of loss per decade of time. For a MLCC having 10uF of capacitance at 1,000 hour and losing 3% of capacity per decade of time, this becomes

$$C(t) = 10 \left[\ 1 - 0.03\, x(t)\ \right]_{t \geq 1000},$$

The Kemet company publishes an Excel spreadsheet [7] which uses this exact formula and a reference (or "referee") time of 1,000 hours.

For a product lifetime of ten years (about 88,000 hours), a 3% aging rate results in a total loss of roughly six percent. If the capacitor's tolerance is ±10%, then one would expect that 10uF capacitor to be no more than 16% down (8.4uF) after ten years. What you aren't told is that's only true if it is operated at zero bias for those ten years.

Models Have Limits

Resist the desire to run these equations backwards in time, prior to 1000 hours. Behavior immediately after annealing is not linear with logarithmic time, and capacitance does not tend to infinity at time zero as the equation suggests.

Some will also notice that for very large values of t, the equation would have capacitance going to zero, then negative. This is obviously impossible, so at some point point in the distant future, the model is also not valid. At what point this happens we don't know. Absent data from tests running for a full ten years, accuracy this equation for long time spans is unknown.

Fatigue

We found no reason to doubt the aging rate specified by manufacturers. A small number of experiments with zero bias suggest the 2 – 3% per decade rate is accurate. But that's not the end of the story. Place an MLCC under DC bias and it will start to lose capacitance at a faster rate. In some cases, a *lot* faster. Our experiments have shown loss rates as high as 15-20% per decade of time depending on bias voltage and time since application of bias.

In addition to initial loss of capacitance under DC bias, and depending on the capacitor and bias voltage, the additional loss in capacitance after ten years under constant bias could be an additional 30% or more. This is based

on behavior we measured out to about 4,500 hours to date. Specifically, we have directly observed an additional 30% loss over 4,500 hours of time due to DC bias on a single 10μF MLCC operated at a bias level within the specified limits.

It's important to note again that this 30% of loss is on top of what's initially lost when DC bias is applied. The 10μF capacitors tested initially dropped to about 7μF under a 6-volt bias, and at the end of 4,500 hours had dropped to less than 5μF. Graphs of this behavior are included later in this article, see figures 15 through 17.

Is It Logarithmic?

It's claimed that both aging and fatigue have a constant slope in logarithmic time. Our measurements of fatigue out to 15,000 hours seem to disprove this claim, as can be seen in figure 16.

One way of estimating the variations in aging rate on a logarithmic time scale is by fitting low-order polynomials to the measured data.

$$C(x) = \sum_{k=0}^{N} C_k \, x^k$$

Estimated aging rates shown in figure 17 are the derivatives of such polynomial fits.

Some discussions of aging (not fatigue) found in documents and on web sites suggest that the first 24 hours or so of aging is not representative or that behavior in this period is *unstable*. Our measurements indicate the following:

- Variations in the first few hours of log-time do have a different slope.
- This behavior is *not* unstable in the sense of wildly varying up and down. Variations are smooth versus log-time right from the start.
- For the ranges of time examined so far (up to 15,000 hours),
  - At low bias levels, capacitance loss accelerates over time. It presumably levels off later, but we don't have data to show that.
  - At higher bias levels, loss rates start out high, then decelerate over time.

Conclusions

These observations and opinions are applicable to designs intended to have lifetimes of several years or longer. For such designs, extreme capacitance values in a given package size should be used with great caution, or completely avoided. Test data suggests that operating MLCCs at bias levels which reduce zero-bias capacitance by no more than 10% may be sufficient to avoid excessive long term losses due to fatigue.

This 10% threshold can be loosely translated to a limit on energy density inside the capacitor. While this is interesting from a theoretical perspective, it is probably best to use the 10% loss threshold when specifying parts.

Additional comments and observations:

- We did not collect enough data to conclude that one manufacturer's parts are in general better than another.
- All capacitors tested exhibit significantly less (10-30%) than rated capacitance at frequencies used in our tests (10 to 100kHz and above). Manufacturers generally specify capacitance at a frequency of 1kHz.
- Sensitivity to DC bias does not seem to correlate well with:
  - Dielectric temperature coefficient – X5R vs X7R
  - Voltage rating
- Energy density seems to be a rough predictor of excessive loss of capacitance under bias.

Derating Examples

Specific recommendations provided below are for Kemet brand capacitors, based on the suggested 10% limit. This should not be construed as an endorsement of Kemet. We do not have an opinion about the quality or performance of Kemet capacitors compared to other brands. The reason we chose Kemet is simple – their K-Sim online simulator tool provides graphs of capacitance versus DC bias and this made it easy to come up with recommended maximum capacitance limits.

Other manufacturers may also provide design tools to predict capacitance as a function of bias so our 10% loss guideline could be applied to that data as well. Lacking that, measurements made with an LCR meter could be used.

Energy density calculations could theoretically be used to set part size limits. However, due to the wide range of densities over which problem behaviors begin to appear, choice of parts using this criteria may not be a reliable technique.

Things can get more complicated in real world situations where more than just second and third source manufacturers for parts are required. When industry capacitor supplies become severely depleted as happens on occasion, second or third sourcing may not be adequate. It could become necessary to research a multitude of manufacturers for a single MLCC and testing samples with an LCR meter might be the best way to qualify a large number sources.

MLCC Selection Guidelines

For those interested in designing products with lifetimes of many years, and based on manufacturer data and our measurements, figure 2 contains some possible guidelines for maximum capacitance in different SMT packages and bias voltages. Also shown in the figure is the energy density in the capacitor at the specified bias voltage (not at the rated voltage), in micro-Joules per cubic millimeter (more on that below). These limits were developed for Kemet brand capacitors in X7R dielectric and is based entirely on data provided by their K-Sim tool. In general, these limits will keep capacitance within 10% of the zero-bias value. Based on our experiments with fatigue, we think this will limit that loss to about 15% or less over a 10-year lifetime under continuous bias. A minimum 2:1 voltage de-rating was used in specifying rated voltages.

Adhering to these limits may prevent the initial capacitance from decreasing by more than 25-30% over a ten year lifetime under bias. There's no guarantees here, this is only our best guess at some reasonable limits.

Bias	0402	0603	0805	1206	1210
3.3	100nF 6.3V	1uF 6.3V	2.2uF 6.3V	4.7uF 6.3V	10uF 6.3V
	2.2	5.3	3.8	4.5	3.6
5	100nF 10V	470nF 10V	2.2uF 10V	3.3uF 6.3V	10uF 10V
	5.0	5.7	8.8	10.4	8.2
9	10nF 25V	220nF 25V	1uF 25V	1.5uF 25V	3.3uF 25V
	1.6	8.7	13.0	7.4	9.5
15	10nF 50V	100nF 50V	100nF 50V	330nF 50V	1uF 50V
	4.5	11.0	7.9	6.5	8.3

Figure 2: Maximum capacitance guidelines with energy density (μJ/mm^3)

In summary, these recommended limits were determined using the 10% threshold for loss under bias, Kemet's K-Sim simulator, and our measurements of fatigue in a 10μF 1210 MLCC. We make the assumption that loss of capacitance under bias is a predictor of fatigue rate.

Energy Density

In analyzing test data, we noticed that there may be something in common with the recommended limits – energy density:

$$D = \frac{CV^2}{2LWT}$$

With C in μF, V in volts and length, width and thickness (L, W, T) in millimeters, the result will be in micro-Joules per cubic millimeter. Published external MLCC dimensions are used for this calculation.

Figures 3 and 4 show the values we used in computing energy density values used in figure 2.

Package	L (mm)	W (mm)
0402	1.0	0.5
0603	1.6	0.8
0805	2.0	1.25
1206	3.2	1.6
1210	3.2	2.5

Figure 3: Part dimensions used to calculate energy density

Using the published exterior dimensions is not ideal because the active volume of dielectric is going to be smaller. This might explain why smaller packages seem to limit out at lower energy densities – if a smaller portion of their total volume is active.

There's enough variation in calculated energy density that this should probably not be used as a hard limit, but densities much above 10-13μJ/mm^3 would warrant concern

DC Bias	0402	0603	0805	1206	1210
3.3	100nF 6.3V 0.5 / 0.25	1uF 6.3V 0.8 / 1.02	2.2uF 6.3V 1.25 / 3.13	6.8uF 10V 1.6 / 8.19	10uF 16V 1.9 / 15.2
5	100nF 10V 0.5 / 0.25	470nF 10V 0.8 / 1.02	2.2uF 10V 1.25 / 3.13	6.8uF 16V 1.6 / 8.19	10uF 16V 1.9 / 15.2
9	10nF 25V 0.5 / 0.25	220nF 25V 0.8 / 1.02	1uF 25V 1.25 / 3.13	1.5uF 25V 1.6 / 8.19	4.7uF 50V 2.5 / 20.0
15	10nF 50V 0.5 / 0.25	100nF 50V 0.8 / 1.02	220nF 50V 1.25 / 3.13	470nF 100V 1.6 / 8.19	1uF 100V 1.7 / 13.6

Figure 4: MLCC thickness (mm) / volume (mm^3)

Supporting Information

Manufacturers also offer one or more series of high reliability MLCCs, for both commercial off-the-shelf (COTS) and military, aerospace and space use (mil-spec). The maximum capacitance values available in these product lines at a

50V rating are not that different than our recommended maximum values in figure 2.

Package	0603	0805	1206	1210
Kemet COTS	150nF	680nF	2.2μF	4.7μF
AVX APS	100nF	1μF	2.2μF	4.7μF
AVX MIL-PRF-32535	180nF	1μF	2.2μF	1.0μF
AVX MIL-PRF-123	n/a	18nF	39nF	100nF

Figure 5: Maximum high-rel capacitor values

Note that MIL-PRF-123 parts are restricted in electrode materials and maximum sizes are smaller due to this. The MIL-PRF-32535 standard was developed to address this issue.

Appendix A – Test Details

A Hewlett-Packard LCR meter was used to explore both dependence of capacitance on bias as well as aging and fatigue behaviors. This included

- HP4275A Option 001
- HP16023B Bias Controller
- Agilent 16034H SMT Test Fixture

This LCR meter appears to implements something like a 4-wire measurement at the front panel – but that's an over-simplification. The SMT test fixture provides a single point of contact at each side of the part under test. The LCR meter provides control over the following parameters:

- Frequency, 10kHz to 10MHz in 1,4,10 sequence
- Signal level continuously variable 1mV to 1V
- DC bias from -35V to +35V

All tests were performed with either a 50mV AC voltage across the capacitor, or a 10mA current through it. With larger capacitance values, the full 50mV cannot be developed across the part and a specific test current is specified instead.

The instrument had not been recently calibrated by the factory when these tests were performed. The meter's performance was sanity-checked using several 2% SMT film capacitors and some 0.1% SMT resistors. These checks provided no cause to suspect the measurements presented below are not valid.

For DC bias dependence, three different values of capacitance were tested, 100nF, 1uF and 10uF. All capacitors had a 10% value tolerance. The results typically show a lower capacitance at zero bias compared to a small bias (e.g. 2-3 volts). This is due to a hysteresis effect; if the bias is held at a large value for some time then returned to zero, measured capacitance will be higher than it initially was, and slowly decreases to the original value over the period of several minutes.

Capacitance was measured at 100kHz for the 100nF values and at 10kHz for larger (1uF and 10uF) units. Manufacturers typically specify capacitance at 1kHz and the LCR meter is not capable of that so it was not possible to verify the rated capacitance.

Fatigue was examined for a single part - 10μF in a 1210 SMT package. This was chosen because it could be biased to energy densities above our proposed limits. This allowed bias levels on both sides of the threshold to be explored in a single part.

Annealing

Measurements of capacitance versus DC bias did not use annealed capacitors. The parts had an unknown amount of aging an fagitue which may be part of the reason many of them appeared to be out of tolerance at zero bias. The other factor is probably that the test frequencies were higher than the nominal 1kHz used by manufacturers to specify the parts.

All capacitors used for fatigue measurements were fully annealed at 300F for at least two hours, and tests were commenced about one hour after cooling to room temperature.

Temperature

For consistent results, it became necessary to track temperature variations during the test runs. Raw readings of capacitance versus time clearly show variations caused by cycling of the building's heating/cooling system. For most of the tests, approximate temperature correction data was generated which largely removed the effect of temperature variations.

Long-Term Tests

A test run begun in November 2019 has provided data spanning a period of roughly 15,000 hours. A combination of AAA and 9-volt alkaline batteries were used to apply bias to four AVX 1210YD106K MLCCs (10μF 16-volt X5R in 1210 SMT package). Voltages were generated by combinations of the following.

- Two AA cells – 3.2 volts
- Four AA cells – 6.4 volts
- One 9V cell – 9.0 volts
- Four AA plus one 9V cell – 15.4 volts

Due to the measurement requirements of the LCR meter, the capacitors are temporarily removed from battery bias during measurement with bias applied

by the LCR meter. We assume the couple of minutes during which the capacitors are unbiased during this process is not significant; the measurements are only performed once every few days in the beginning, much less frequently later on.

Appendix B – Measurement Results

The first set of results below show variation of capacitance with bias over short periods of time. An AVX 10μF capacitor in 1210 SMT package is examined in a little more detail.

Graphs are presented with Y-axes showing absolute capacitance and capacitance relative the the maximum value for three different MLCC parts.

Variation of Capacitance with Applied Bias

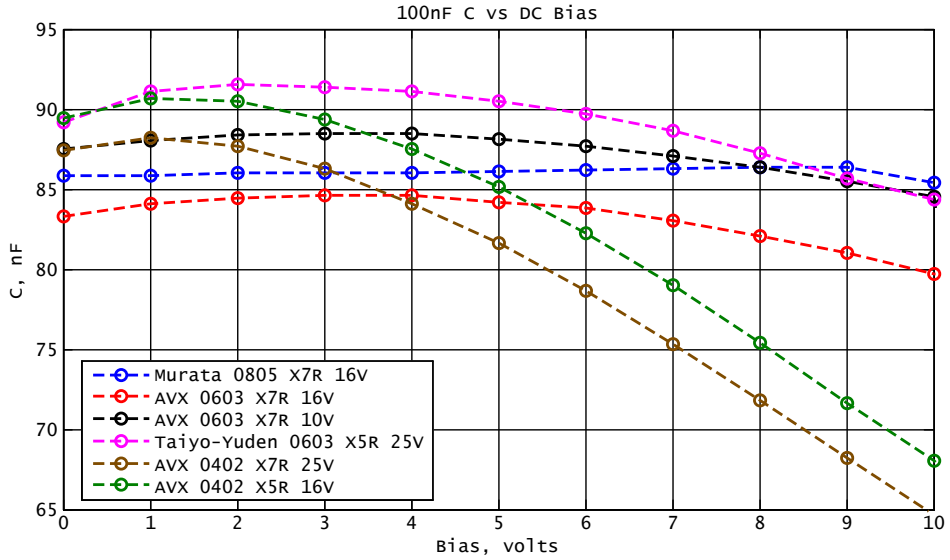


Figure 6: 100nF Absolute Capacitance

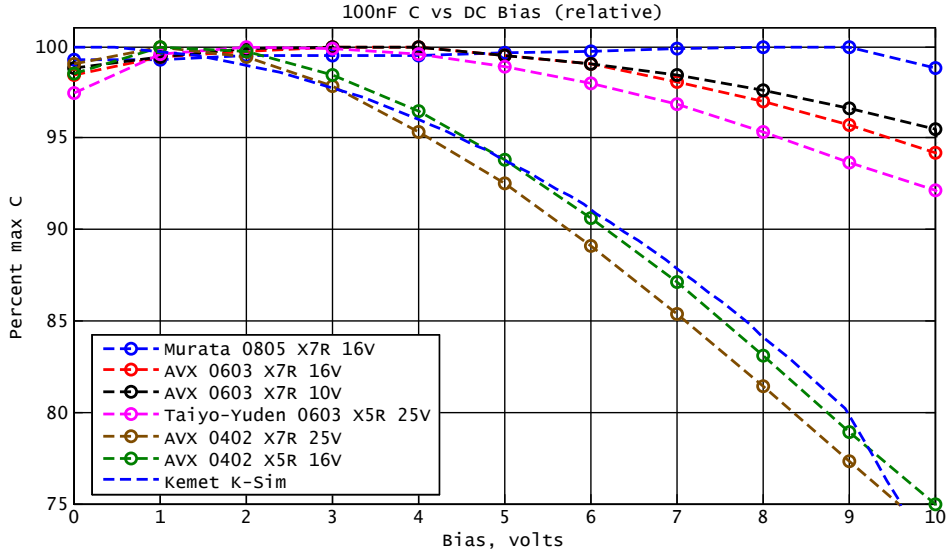


Figure 7: 100nF Relative Capacitance

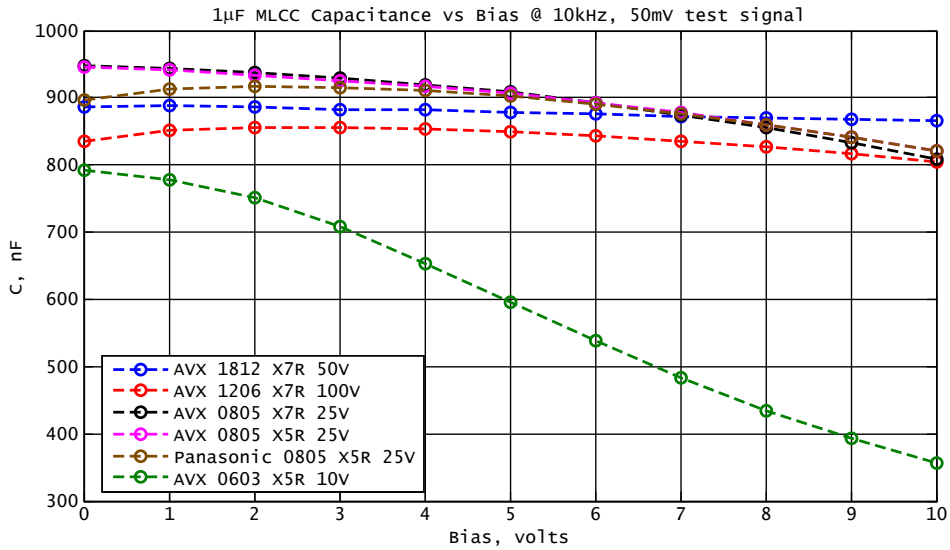


Figure 8: 1uF Absolute Capacitance

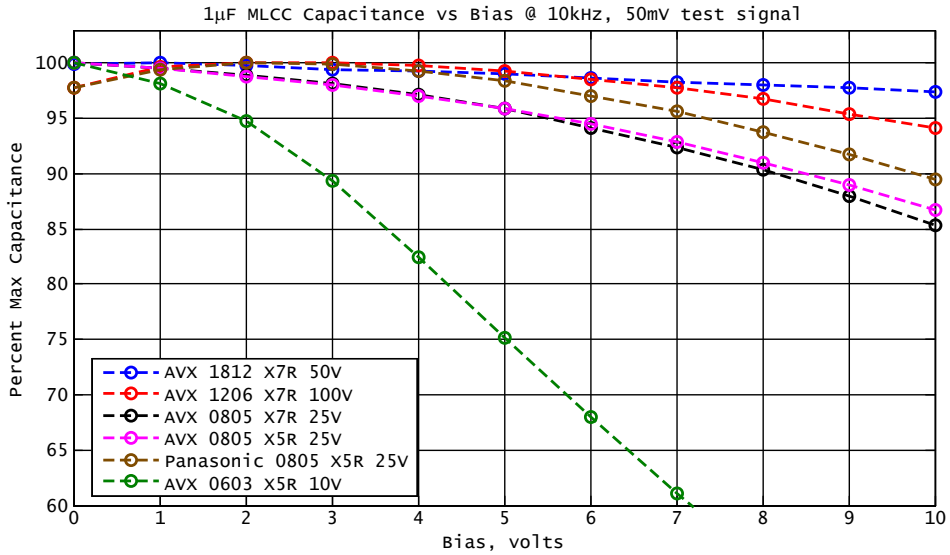


Figure 9: 1uF Relative Capacitance

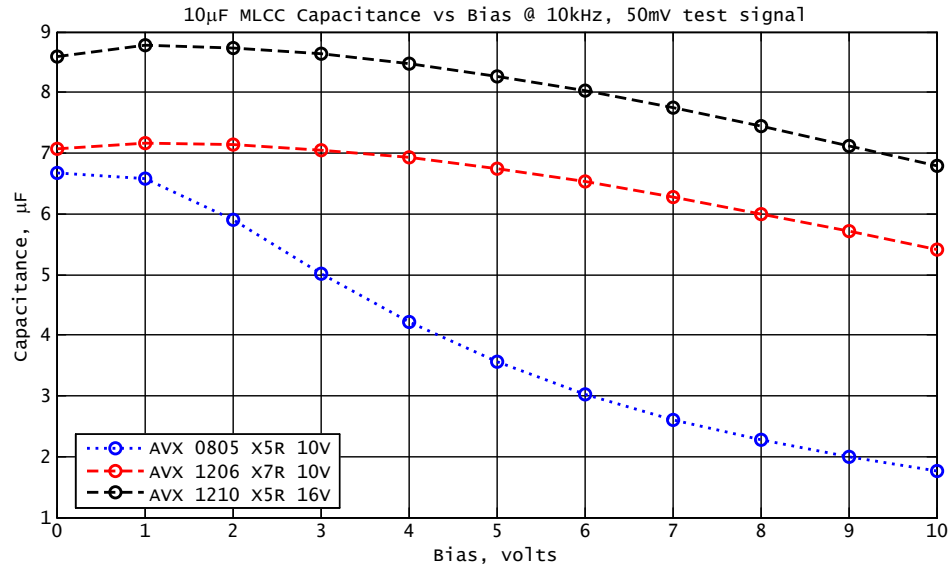


Figure 10: 10uF Absolute Capacitance

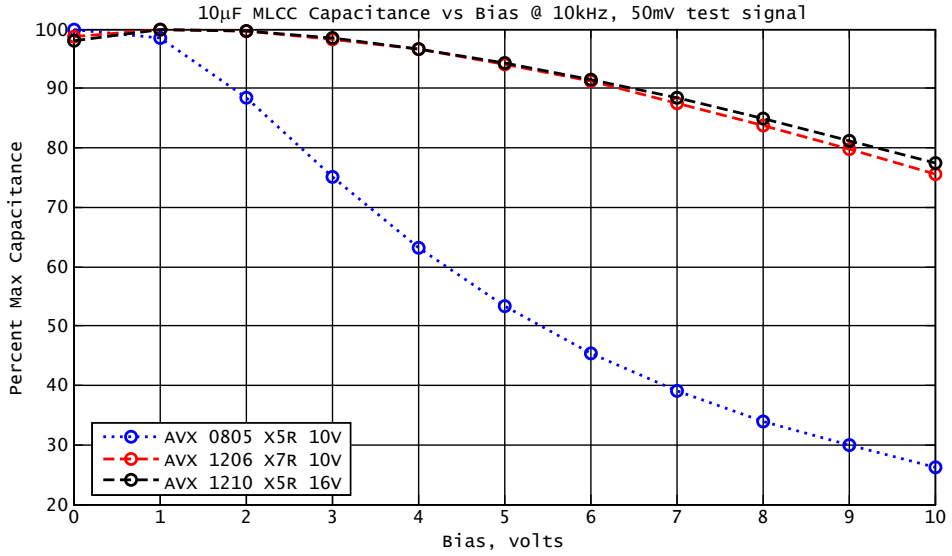


Figure 11: 10uF Relative Capacitance

A Detailed Look at the AVX 1210YD106K

Figures 12 and 13 provide a more detailed look at one specific part, an AVX 10uF 16V X5R MLCC in the 1210 package size. This covers the full bias range up to 16 volts.

At each measurement point, the capacitor was allowed to settle for at least a couple of minutes before recording the value. Because of ongoing fatigue (especially at higher bias values), these measurements should only be considered approximate.

Three measurements of the same physical part are shown. The first two (blue and red) are different runs starting at zero and incrementing in one volt steps up to 16 volts. The last measurement (black) started after the red measurement, and stepped down one volt at a time to zero volts. Differences in the runs are likely a combination of hysteresis and fatigue.

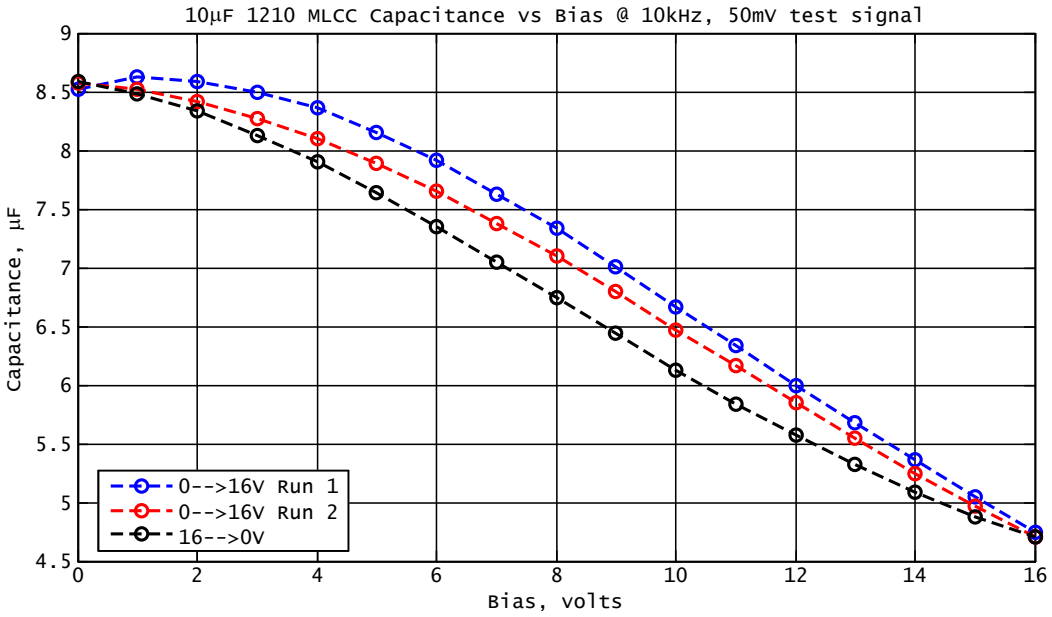


Figure 12: AVX 10uF 16V 1210 MLCC

Figure 13 has the capacitance values scaled such that 100% represents 8.62uF. It also includes the bias dependence output by Kemet's K-Sim on-line simulator. This is comparing an AVX part to a Kemet simulation. Up to about 9 volts, the agreement is excellent. The Kemet data has a breakpoint at about 9 volts, after which the slope becomes increasingly negative and provides an overly pessimistic estimate of capacitance above 10-11 volts or so. At the

rated voltage of 16 volts, the K-Sim estimate is low by about 9.2%, predicting 3.92uF versus a measured value of 4.71uF.

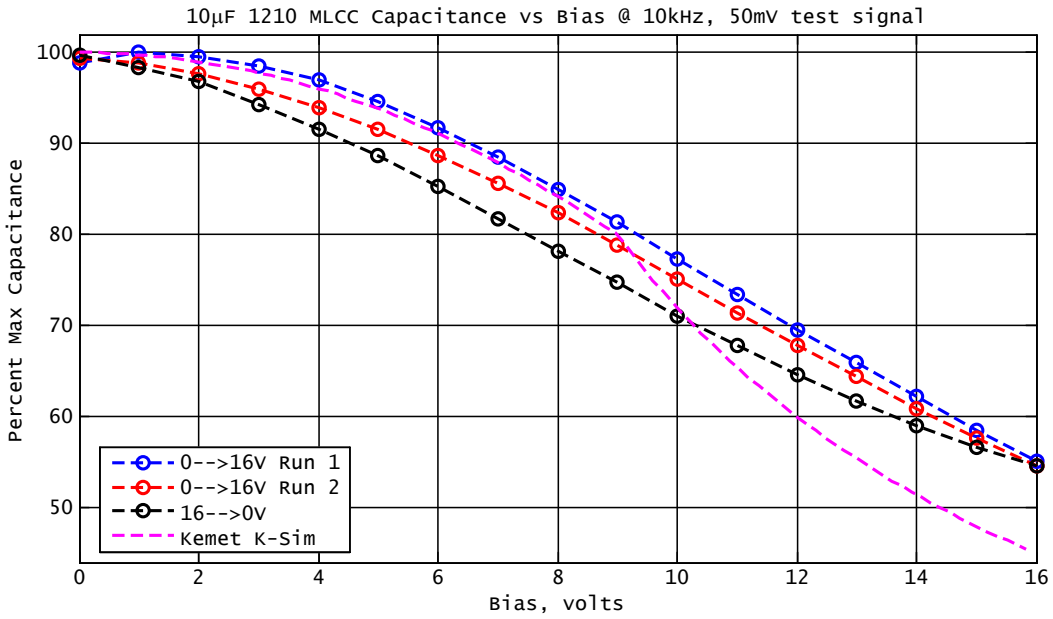


Figure 13: AVX 10uF 16V 1210 MLCC

The discrepancy between the Kemet model and AVX part in figure 13 (at bias voltages above 9 volts) may be an attempt by Kemet to allow for fatigue, but that's just a guess. If that is indeed the case, it's not a very good estimate as evidenced in figure 15, where capacitance at 16V bias drops to nearly 3μF (or about 34% of maximum capacitance) after being biased for a little over 300 hours. The data shown in figure 15 is for an AVX part, so it may not be fair to compare it to the K-Sim data.

Aging and Fatigue Measurements

Measurements were made using the same physical part for a variety of different bias levels. These results are shown in figure 14.

Bias	C(1hr) μF	nF/decade	%/decade	Time (hrs)	Trend
0V	9.4	90-140	1-1.5	65	Incr
4V	8.96	165	1.8	14	Incr
6V	8.42	340	4.0	41	Incr
8V	7.75	1160	15	390	Flat
16V	4.4	260	6	340	Decr

Figure 14: Measured Fatigue Rates (single part)

In figure 14, the run at zero bias was dominated by temperature noise and the aging rate shown is subject to quite a bit of uncertainty. Rates as percentages are computed using the capacitance approximately one hour after being initially placed under bias. This gives a more favorable number than if the value after a longer time (e.g. one day) was used.

In all except one case (8-volt bias), the rate of loss was either accelerating or decelerating at the end of the test. As a result, using these values for longer term behavior is of questionable value.

What is unquestionable however, is that assuming an aging rate of 2-3% per decade for MLCCs under constant bias is not necessarily accurate.

Long Term Test Results

Four different physical samples were placed under four different levels of constant DC bias for 420 days – just over 10,000 hours. The capacitors tested were AVX 10μF 16-volt MLCCs in a 1210 package (AVX part number 1210YC106K). We want to stress here that we are aware of no reason to suspect MLCCs from other manufacturers will behave much differently.

Figures 15, 16 and 17 show the measured loss of capacitance during this test run. Figure 16 makes it easy to see that for smaller bias voltages, loss starts out slow, then accelerates. At high bias (16V), loss starts out fast (about 15% per decade of time), then begins slowing after about 100 hours. This makes us wonder if the data for lower bias values would behave similarly on expanded time scales. This would make sense if the mechanisms causing loss of capacitance are the same regardless of bias level.

Parts under bias of at least 6.4 volts seem to have leveled out at the 10,000

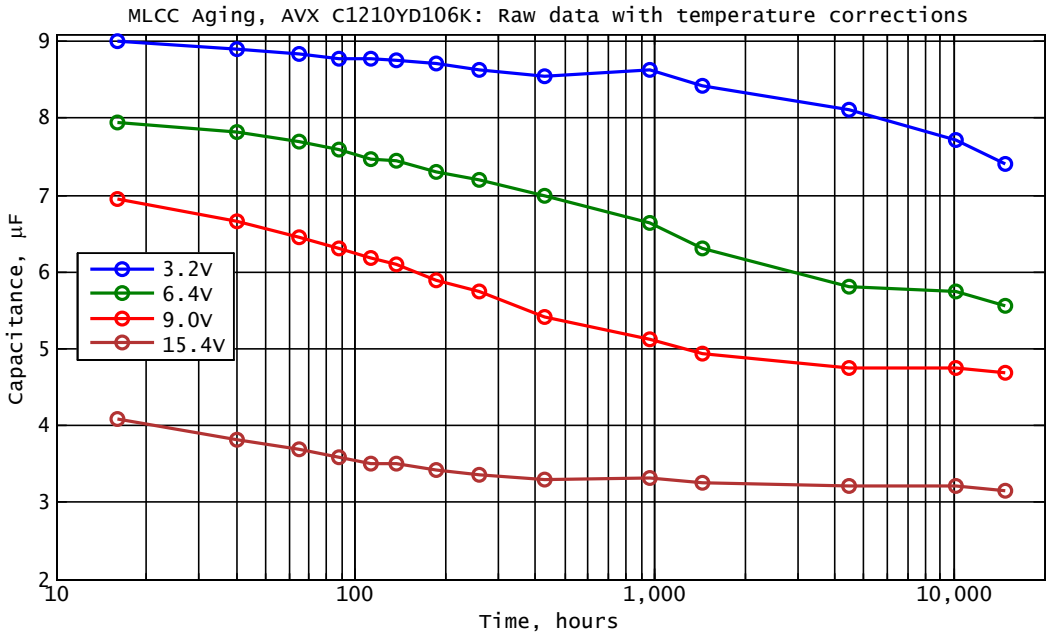


Figure 15: 10uF 16V 1210 MLCC Fatigue Measurements

hour mark, while the part under 3.2 volt bias is showing continued loss, although the rate seems to have leveled off.

In figure 16 it is apparent that losses under bias which has leveled off at 10,000 hours (6 volts bias and above) show differing amounts of loss compared to initial loss. This percentage is least under 15V bias and worst under 9V bias, with the 6V part somewhere in between. The inconsistency here provides no help in guessing where the part under 3V bias will eventually level off.

Figure 17 shows rates of loss (percent per decade of time) relative to the initial capacitance, which is determined about one hour after applying bias after the oven annealing procedure. For example, the rate for 16 volts bias is relative to an initial capacitance of about 4.4μF.

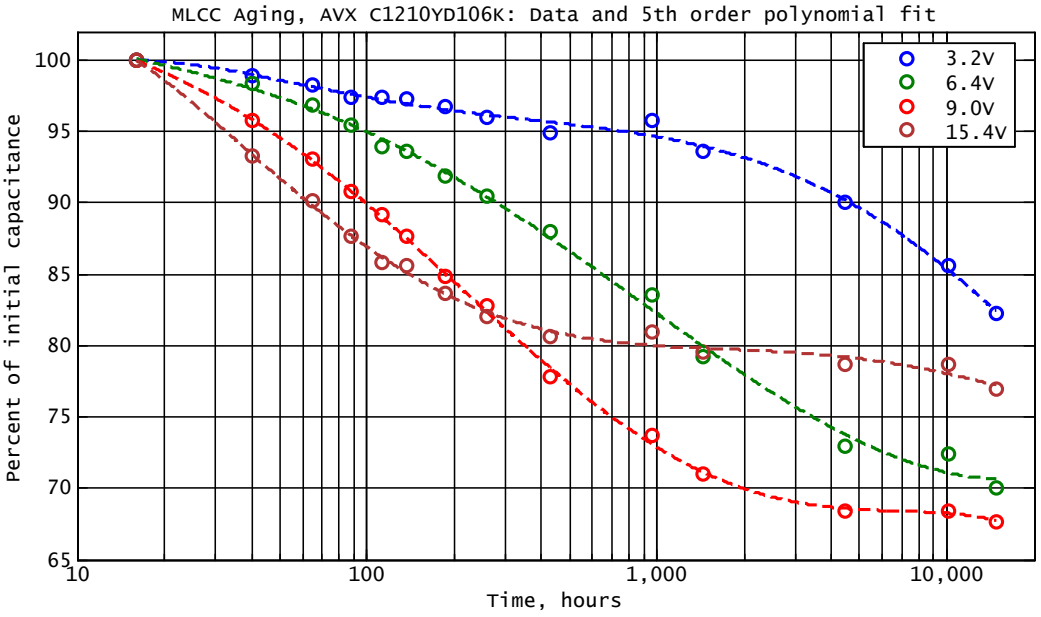


Figure 16: 10uF 16V 1210 MLCC Relative Fatigue

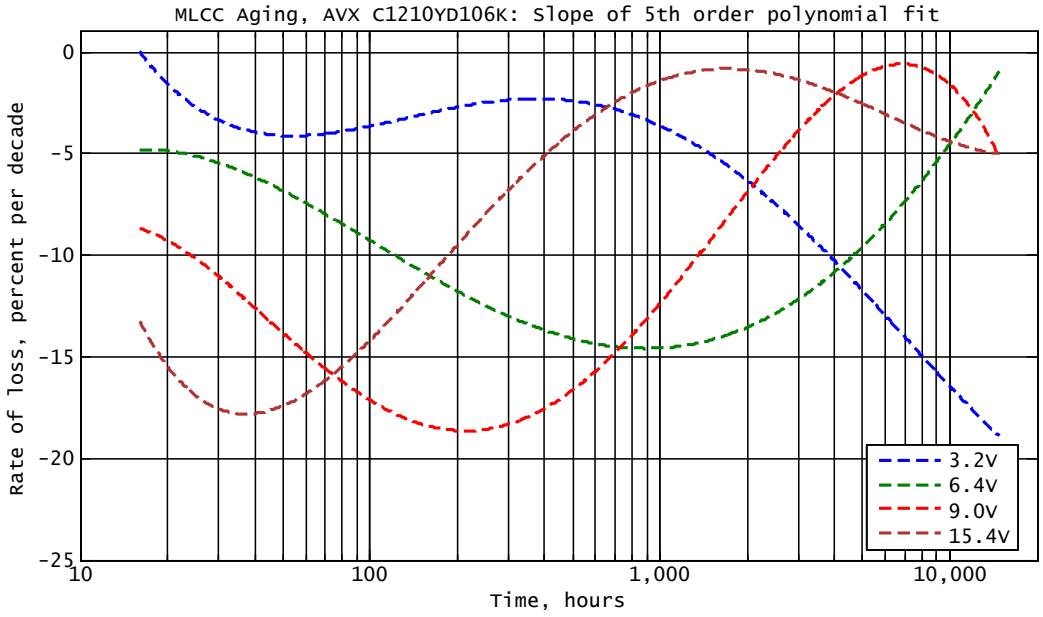


Figure 17: 10uF 16V 1210 MLCC Fatigue Rate Estimates

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